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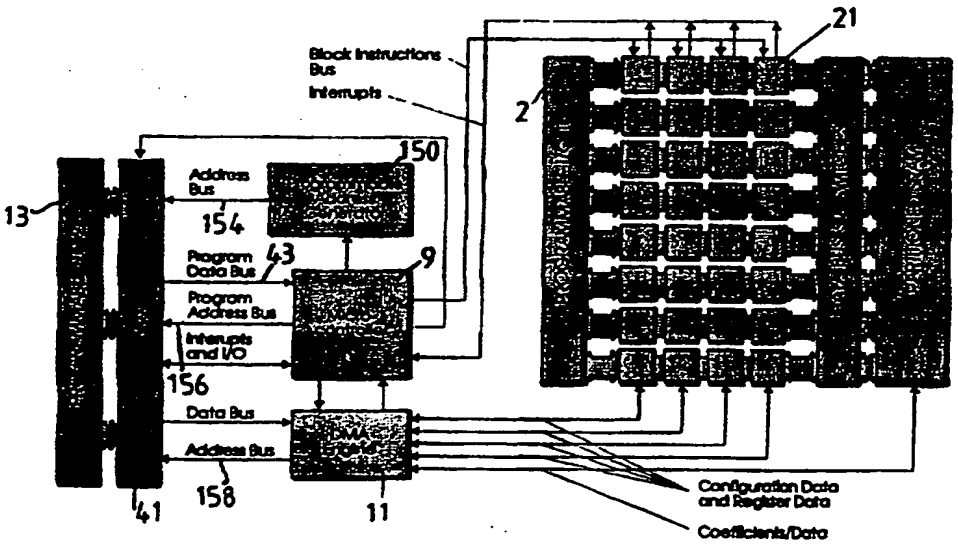
(54) Title: RE-CONFIGURABLE APPLICATION SPECIFIC DEVICE



(57) Abstract

In a re-configurable semi-conductor integrated circuit device which, as made, comprises a plurality of cells (2) which have two or more possible configurations, means (3) for storing configuration data for at least two cell configurations (per cell), data memory (5) for the array of cells, and input/output channels for the device, improvements in flexibility and efficiency are made possible by the provision of a programmable micro-controller (9) and a direct memory access engine (11) controlled by the programmable micro-controller to control the transfer of data to and/or from: the array memory; the input/output channels and the means storing configuration data. Re-configuration may be initiated by interrupt signals generated by an off-chip signal, an on-chip signal or an on-chip event. A plurality of programmable sequencers are used to generate a sequence of configuration data storage addresses.

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TITLE: Re-configurable application specific device

DESCRIPTION

The present invention relates to a re-configurable integrated circuit, with particular emphasis on a re-configurable application specific device, but without limitation to same.

U.K. Patent Application No. 9503003 describes a configurable semi-conductor integrated circuit, eg. a digital signal processor, in which an area thereof is formed with a plurality of cells each having at least one function and interconnections with at least some other said cells. At least some of the plurality of cells have interconnections which are electrically selectable as to their conduction state, and at least some of the plurality of cells have interconnections which are pre-wired. Each cell has two or more possible configurations, each configuration being defined by the cell function and/or its interconnection with other cells according to cell configuration data. Means is provided for storing configuration data for at least two cell configurations (per cell) and means is provided to enable one of the possible cell configurations according to the cell configuration data selected. A control circuit is utilised to pass configuration data, program

data and coefficients to an array memory and memory caches.

The previous architecture had fixed programming circuitry and the present invention aims to provide improvements in flexibility and efficiency.

Accordingly, the present invention provides a re-configurable semi-conductor integrated circuit device of the type which, as made, comprises a plurality of cells which have two or more possible configurations, means for storing configuration data for at least two cell configurations (per cell), data memory for the array and input/output channels for the device, the device further comprising a programmable micro-controller and a direct memory access engine controlled by the programmable micro-controller to control the transfer of data to and/or from:- the array memory; the input/output channels and the means storing configuration data.

More particularly, the direct memory engine (hereinafter referred to as a DMA engine) directly generates internal and external addresses transferring a preselected number of data words. Thus, the micro-controller directs data transfer, while the DMA engine is responsible for transferring data at high speed. It receives its instructions from the micro-controller and transfers data in the background.

A further advantageous feature is the provision

of interrupt logic that can be used to interrupt the main flow of data and cause a new set of transfers to occur. Interrupts may be generated either by an off-chip signal, and on-chip signal or an on-chip event caused by an interrupt timer. It is preferred that the micro-controller has a dedicated interrupt circuit for each of the logic blocks. For this purpose each logic block feeds a control node of the micro-processor which can be used to signify the end of a task or request for more data etc. More preferably still, the micro-controller has a timer for each logic block and the timer can be used to time a process that the block is performing thereby freeing the block from dedicating some of its cells to this task. A further alternative is for external signals to be routed into the micro-controller from the input to replace or be used in conjunction with internally generated interrupts.

More particularly the device further comprises a plurality of programmable sequencers which can be programmed individually or in combination to generate a sequence of configuration data storage addresses.

A further feature of the invention comprises a programmable input/output by which the band width allocated for user input/output of configuration data and program data can be altered according to the application of the device.

The present invention will now be described further, by way of example only, with reference to the accompanying drawings; in which:-

Figure 1 is a schematic block diagram showing the principal elements of an integrated circuit device according to the present invention,

Figure 2 illustrates the device of Figure 1 in further detail,

Figure 3 is a schematic diagram showing in further detail one cell of the logic block for the device of Figures 1 and 2,

Figure 4 is a schematic illustrating the logic blocks and the associated circuitry with address line and active cache selection,

Figure 5 is a schematic of the logic blocks showing the details of the circuitry utilised for selecting and updating the memory caches,

Figure 6 is a block diagram illustrating a single bit sequencer for use in the device of Figures 1 and 2,

Figure 7 is a schematic circuit diagram for a programmable modulo counter as used in the single bit sequencer,

Figure 8 is a flow chart illustrating part of a normal program flow, and

Figure 9 is a flow chart showing the interrupt service routine.

The present invention is described in the context of an integrated circuit intended for an application specific device, one embodiment of which is a reconfigurable signal processor (DSP). A device according to Figure 1 comprises a plurality of logic function units or cells 2, programmable inputs and outputs 4 for the logic function units, and a configuration cache 3 storing configuration data for the logic function units. In practice, the configuration cache 3 may be on-chip in immediate proximity to the logic function units as part of an array of logic blocks, as illustrated in Figures 3, 4 and 5. The processor also comprises a data memory 5, a micro-sequencer 7, a micro-controller 9, a direct memory access engine 11 and programmable input/output 13 for the DMA engine and micro-controller.

According to a preferred embodiment the logic block array comprises 32 logic blocks 21 as shown diagrammatically in Figure 2. Each logic block 21 comprises a matrix array of cells, for example an array of 8 x 8 cell. Figure 3 illustrates schematically in further detail one of the logic cells of one of the logic blocks 21. It comprises a cell function unit 22 incorporating the desired logic circuitry, an 8 bit decoder 23, four-8 bit configuration caches 25(a-d), comprising programmable memory (RAM), two-8 bit ROM

configuration memories 27a, b representing two alternative boot-up configurations for the cell function unit. Usually the cells will be disposed in groups, eg. columns which show the same boot up configuration - representing primary functions, eg. shifter, compare, adder etc. Also there are decode cells, eg. the row of cells at the bottom in Figures 4 and 5. Also illustrated are two 4-1 input multiplexers 28, 29 receiving signal inputs from other cells at 38 and 40, and a 1-4 output multiplexer 31 giving outputs to other cells at 42. The decoder 23 controls the input and output multiplexers and the cell function unit, either in terms of logic function or interconnect function by way of connection lines 30, 32, 34 and 36, according to which of the configuration caches 25a-d, 27a, b is selected. In addition an instruction bus 35 connects into the logical unit from the decode cells and also serves to control the function of the logic function unit. In the illustrated embodiment caches 25 and 27 have four and two address lines respectively. Addressing of the logic block and transferring of data is described further with reference to Figure 2, 4 and 5.

The micro-controller 9 instructs the DMA engine 11 having taken its program instructions from the programmable input 13 via multiplexer 41. The program

data is read in along program data bus 43.

Figure 6 illustrates one of eight single bit sequencers for the device which make up the micro-sequencer 7 of Figure 1. Each comprises, in the illustrated embodiment a four-input multiplexer 601 receiving global clock inputs - CLK1, CLK2, CLK3 and CLK4. There are two modulo counters, one, 100, operating on frequency and the other, 101, operating on sequence length. These are set from the micro-controller. A sequence can be stored in each of RAM blocks A and B. Means is provided for selecting which of the sequences is to be output on a global cache line. Figure 6 illustrates the output for global cache-line G1. Thus, there are eight possible outputs G1-G8 for the whole device. The global lines G1-G8 are illustrated in Figure 4. Signals from the 8 global lines can be fed to each logic block 21. The global lines connect with 3, 8 input multiplexer 105, 107 and 109. The micro-controller controls the multiplexers 105, 107, 109 according to the selection of either RAM A or RAM B which has associated read enable, write enable, and data transmission lines 210, 212 and 214 respectively. Outputs from the three multiplexers 105, 107, 109 feed to decoder 115. Furthermore, there are node connections in each logic block and global connections with each logic block, x busses, these can

provide a signal source for selection by the multiplexer as an alternative to or in addition to signals on lines G1-G8. Decoder 15 has six output lines which connect with the respective RAM and ROM memory caches by horizontal connection lines.

Figure 5 illustrates for one logic block the circuitry utilised for selecting and/or updating the caches of the array of cells. Co-ordinate selection of any of the caches 25a-d, 27a, b of a cell is possible utilising the two decoders 502, 504 by way of the DMA engine 11 under the instructions from the micro-controller. Transferring of data to the selected caches (in the case of the RAM caches 25a-d) is by data bus 506 with data being passed by the DMA engine under instruction from the micro-controller. Where the data is to be written to the number of the caches is to be same, this can be written simultaneously to these caches.

The micro-controller has associated interrupt logic which can be used to interrupt the main flow of data and cause a new set of transfers to occur. Interrupts may be generated by either an off-chip signal, for example through the programmable input 13, an on-chip signal or an on-chip event caused by an interrupt timer. The micro-controller 9 has a dedicated interrupt circuitry for each of the 32 array blocks.

Furthermore each block can generate in interrupt by taking a control node on the micro-controller high, signalling the end of a task or request for more data. Alternatively, the micro-controller can use one of its 32 timers (not illustrated), ie. one for each logic block, to time a process that the block is performing thereby freeing the block from dedicating some of its cells to this task. External signals can be routed into the micro-controller which can replace or be used in conjunction with other generated interrupts.

A further feature of the invention is the use of programmable input/output which allows the designer to allocate pins, ie. band width, to apportion user input/output for configuration data and program data. Accordingly, a program address generator 150 is provided - see Figure 2. A multiplexer 41 sets the band width for the configuration data and the program data under control of the micro-controller 9, in conjunction with the DMA engine and the respective address busses 154, 156 and 158. Thus, the band width/number of pins allocated to configuration and program data respectively can be allocated according to the requirements for the task to be performed.

The operation of the circuit will now be described with reference to the flow chart of Figure 8. On powering up the device to configure a specific

application, the program input determines whether one of the prewired ROM configuration 27a, 27b is to be selected. If it is then the required control information is sent to the array as indicated by box 100. If not, then the required configuration data is written to say the first memory cache 25a and the first logic block. The timer will be set for that logic block as will the interrupts for that logic block. The process is repeated for all the logic blocks with the configuration data to be written to the blocks being determined by the architecture specification data, whilst the timers and interrupts are set according to control flow information. This all serves to initialise the array with the required start-up configuration if it is not to be one of the prewired boot configurations. In the normal program flow the micro-controller is programmed to monitor a node in each logic block so that when an event occurs which turns it high or low a corresponding instruction will be carried out. In the example given for a false signal, instructions are sent to a decode cell to set a desired function for one column of cells. That selection will remain, for example until the allocated time has been completed or until an interrupt signal is received from one or more of the various sources. Where the signal is true then an alternative configuration cache is adopted. The

program continues to run with that configuration cache until it is instructed to change caches as part of the program run or according to interrupts.

Figure 9 illustrates a interrupt service routine in more detail from which it will be seen that interrupts may be array interrupts 61 or timer interrupts 63. There is one for each logic block.

CLAIMS

1. A re-configurable semi-conductor integrated circuit device of the type which, as made, comprises a plurality of cells (2) which have two or more possible configurations, means (3) for storing configuration data for at least two cell configurations (per cell), data memory (5) for the array and input/output channels for the device, characterised in that the device further comprises a programmable micro-controller (9) and a direct memory access engine (11) controlled by the programmable micro-controller to control the transfer of data to and/or from:- the array memory; the input/output channels and the means storing configuration data.

2. A device as claimed in claim 1 in which the direct memory engine directly generates internal and external addresses transferring a preselected number of data words.

3. A device as claimed in claim 1 or 2 in which the micro-controller directs data transfer, while the DMA engine is responsible for transferring data at high speed.

4. A device as claimed in any one of claims 1, 2 or 3 in which interrupt logic is provided to interrupt the main flow of data and cause a new set of transfers to

occur.

5. A device as claimed in claim 4 in which interrupts are generated either by an off-chip signal, an on-chip signal or an on-chip event caused by an interrupt timer.

6. A device as claimed in claim 4 or 5 in which the micro-controller has a dedicated interrupt circuit for each of the logic blocks.

7. A device as claimed in claim 6 in which each logic block feeds a control node of the micro-processor which can be used to signify the end of a task or request for more data etc.

8. A device as claimed in any one of claims 4, 5, 6 or 7 in which the micro-controller has a timer for each logic block and the timer can be used to time a process that the block is performing.

9. A device as claimed in any one of claims 4 to 8 in which external interrupt signals are routed into the micro-controller from the input to replace or be used in conjunction with internally generated interrupts.

10. A device as claimed in any one of the preceding claims further comprising a plurality of programmable sequencers which can be programmed individually or in combination to generate a sequence of configuration data storage addresses.

11. A device as claimed in any one of the preceding

claims further comprising a programmable input/output by which the band width allocated for user input/output of configuration data and program data can be altered according to the application of the device.

12. A device constructed and arranged substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

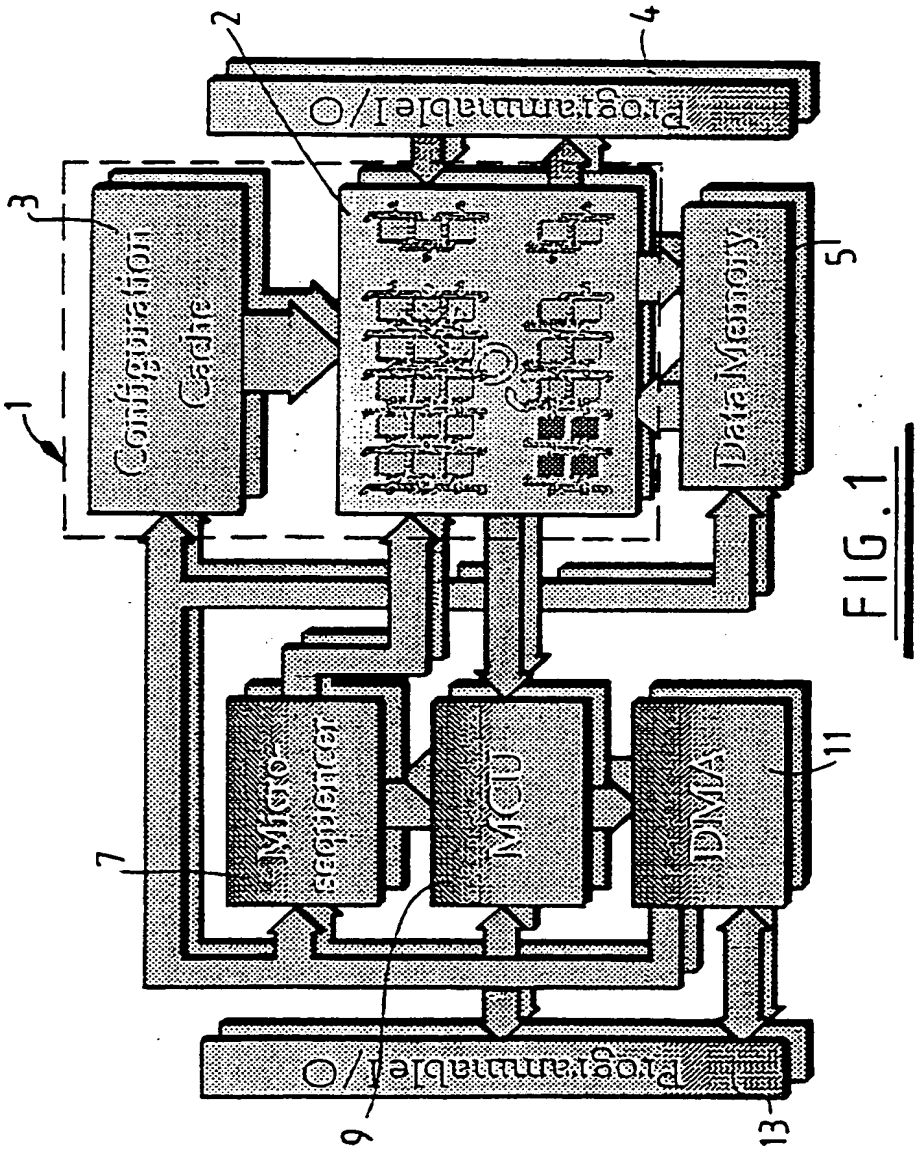
Programmable I/O
Configuration Cache
CPU
Data Memory
Sequencer
MCU
DMA
Programmable I/O
1
2
3
4
5
7
9
11
13

FIG. 1

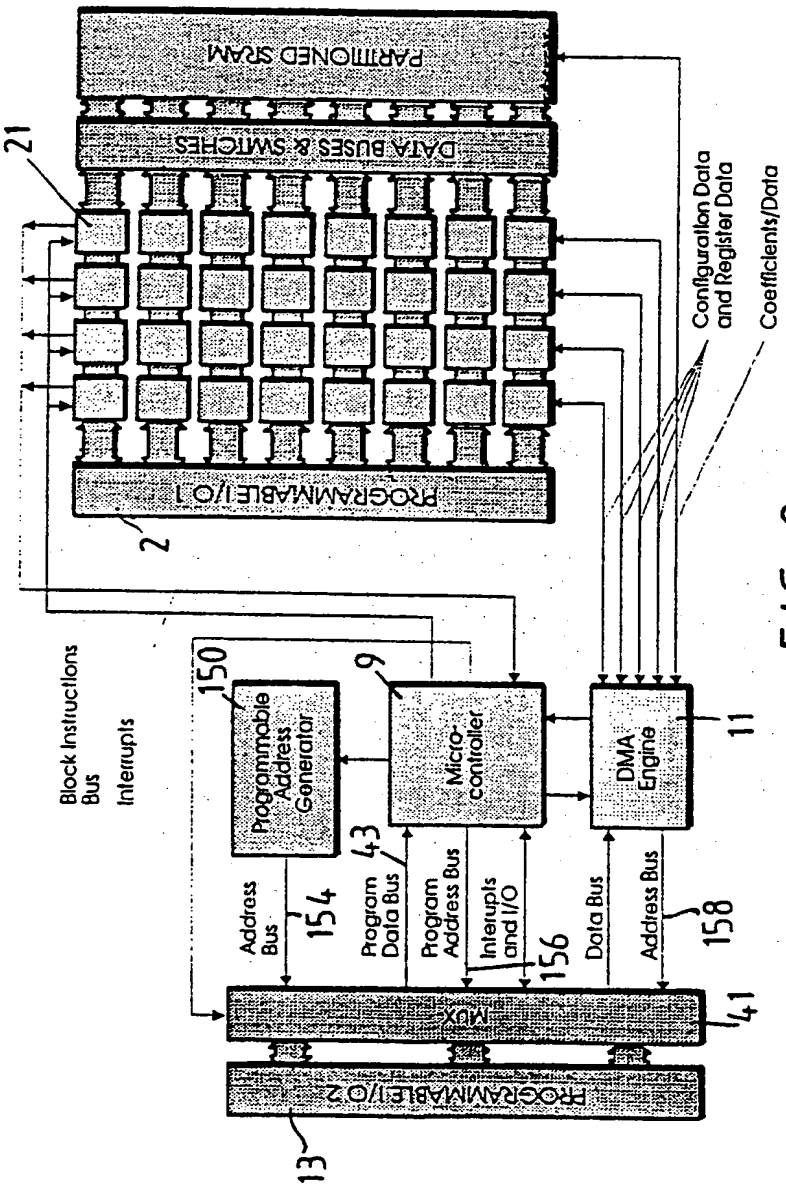
PARTITIONED SRAM
DATA BUSES & SWITCHES
21
PROGRAMMABLE I/O 1
2
Configuration Data and Register Data
Coefficients/Data
Block Instructions Bus
Interrupts
150
Programmable Address Generator
9
Micro-controller
DMA Engine
11
43
Address Bus
154
Program Data Bus
Program Address Bus
Interrupts and I/O
156
Data Bus
Address Bus
158
MUX
41
PROGRAMMABLE I/O 2
13

FIG. 2

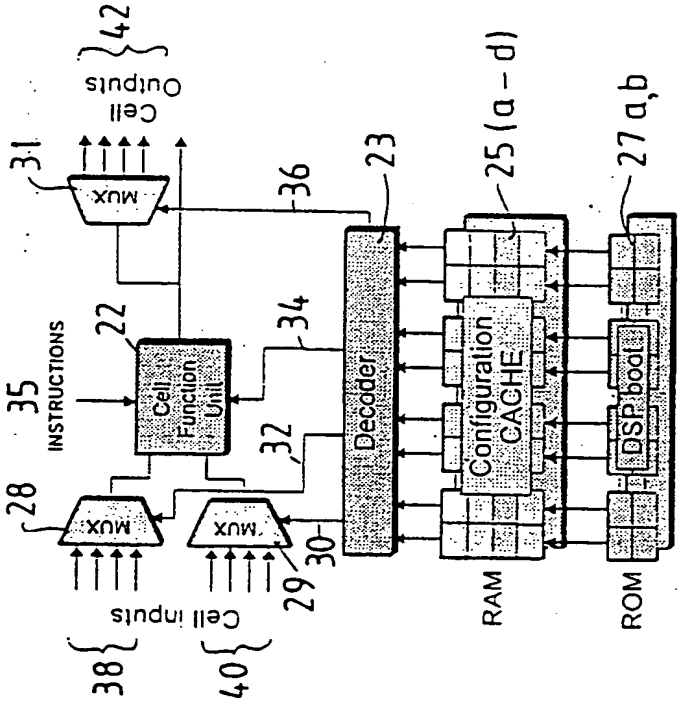
42
Cell Outputs
31
MUX
36
23
25 (a - d)
27 a,b
22
34
35
INSTRUCTIONS
Cell Function Unit
Decoder
Configuration CACHE
DSP boot
32
28
MUX
MUX
30
29
Cell inputs
RAM
ROM
38
40

FIG. 3

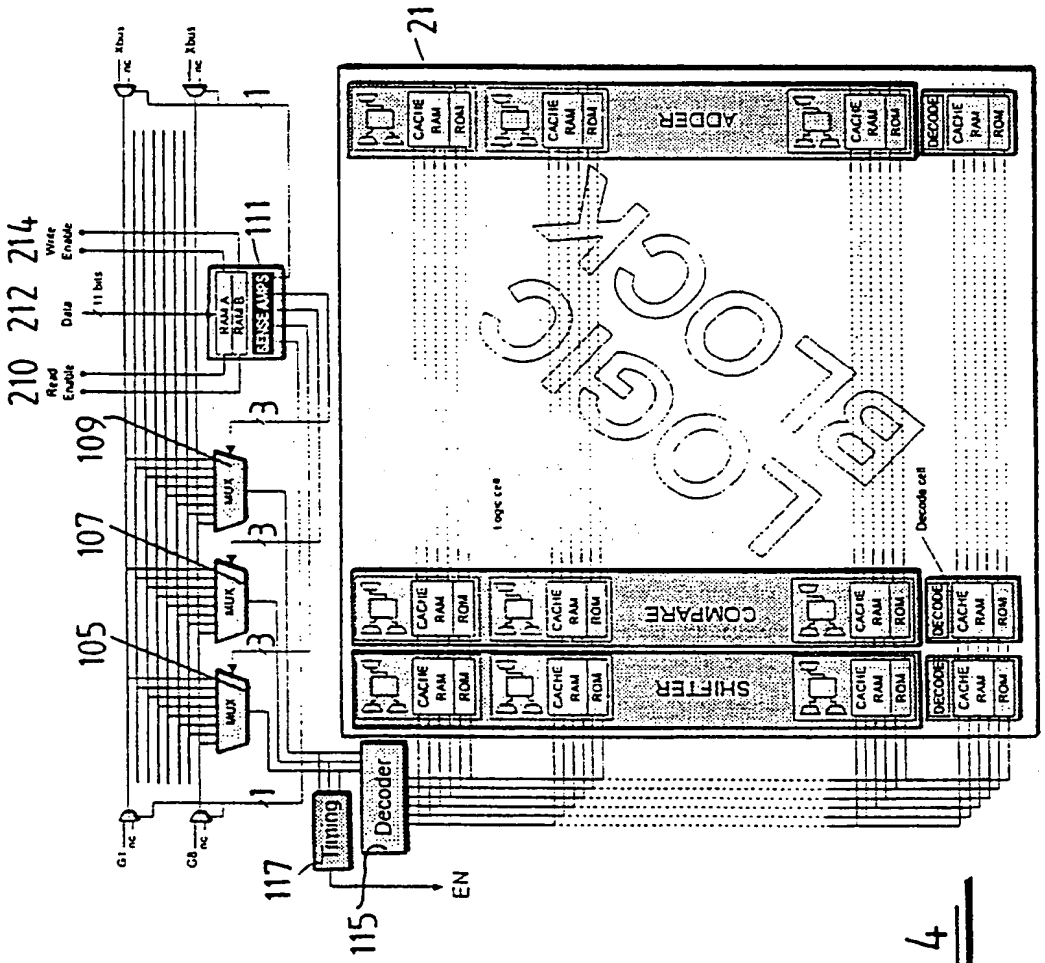
21
1
111
214
212
210
109
107
105
117
115
EN
Xbus
Write Enable
Data
Read Enable
111 bits
RAM A
RAM B
SENSE AMPS
MUX
Timing
Decoder
ADDER
COMPARE
SHIFTER
CACHE
RAM
ROM
DECODE
Logic cell
Decode cell

FIG. 4

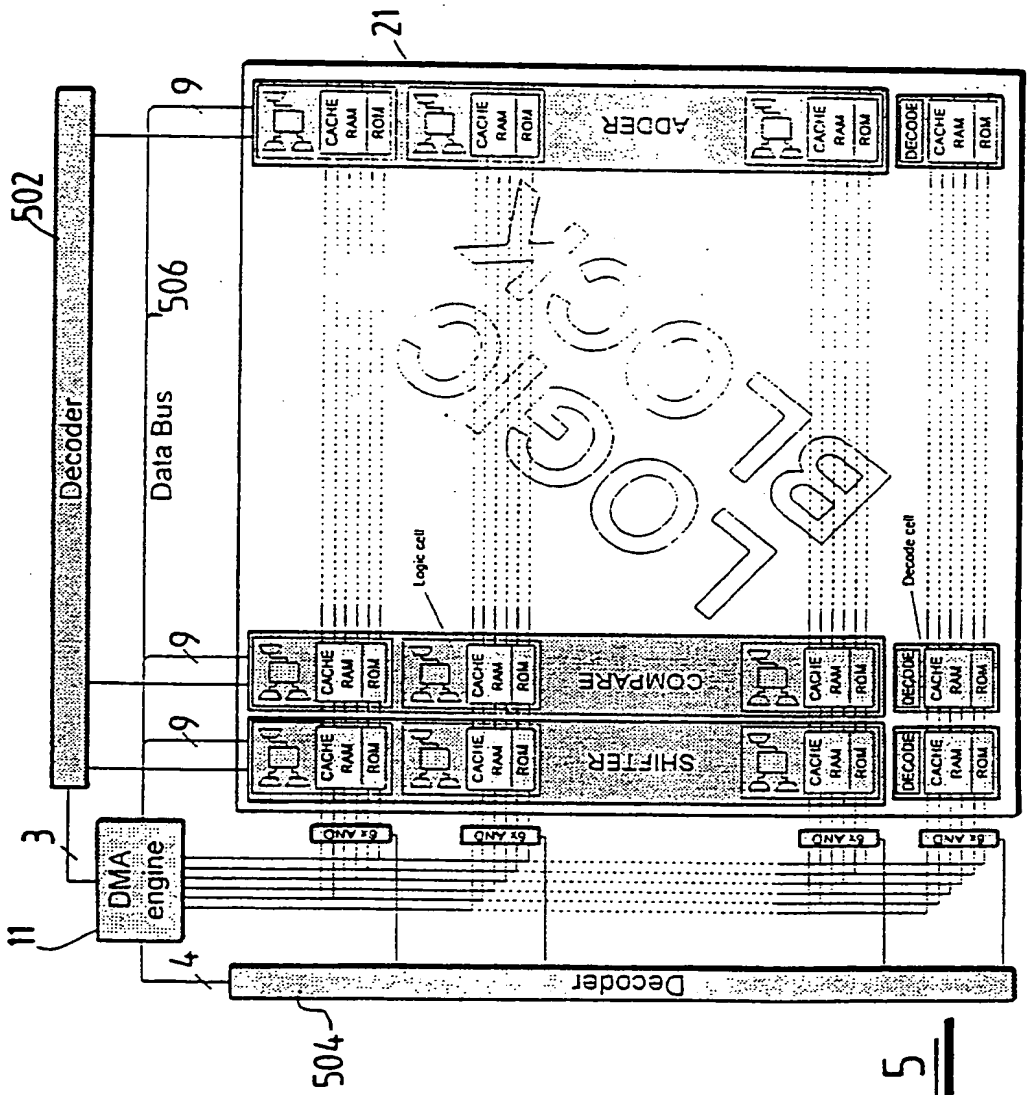
21
9
502
506
Decoder
Data Bus
ADDER
COMPARE
SHIFTER
CACHE
RAM
ROM
DECODE
Logic cell
Decode cell
3
DMA engine
11
4
Decoder
504

FIG. 5

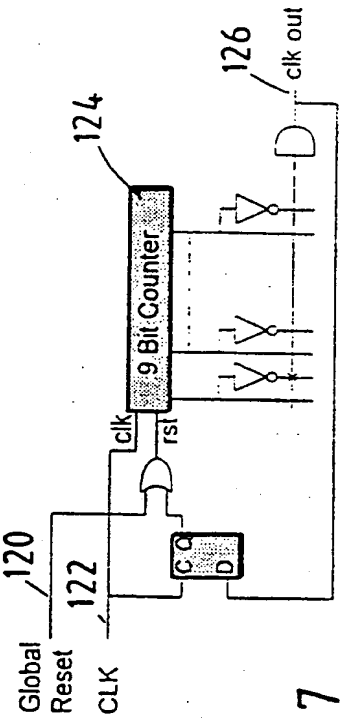
Global Reset
CLK
120
122
124
9 Bit Counter
clk
rst
C Q
D
126
clk out
D

FIG. 7

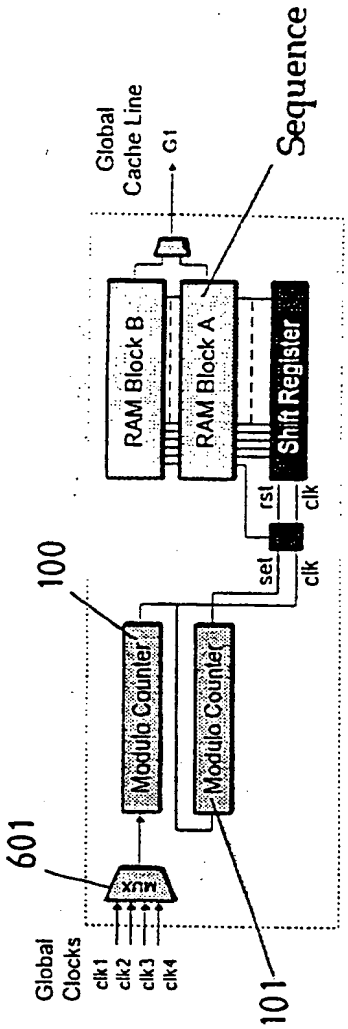
Global Clocks
clk1
clk2
clk3
clk4
601
MUX
100
Modulo Counter
Modulo Counter
101
Global Cache Line
G1
RAM Block B
RAM Block A
Shift Register
Sequence
set
rst
clk
clk

FIG. 6

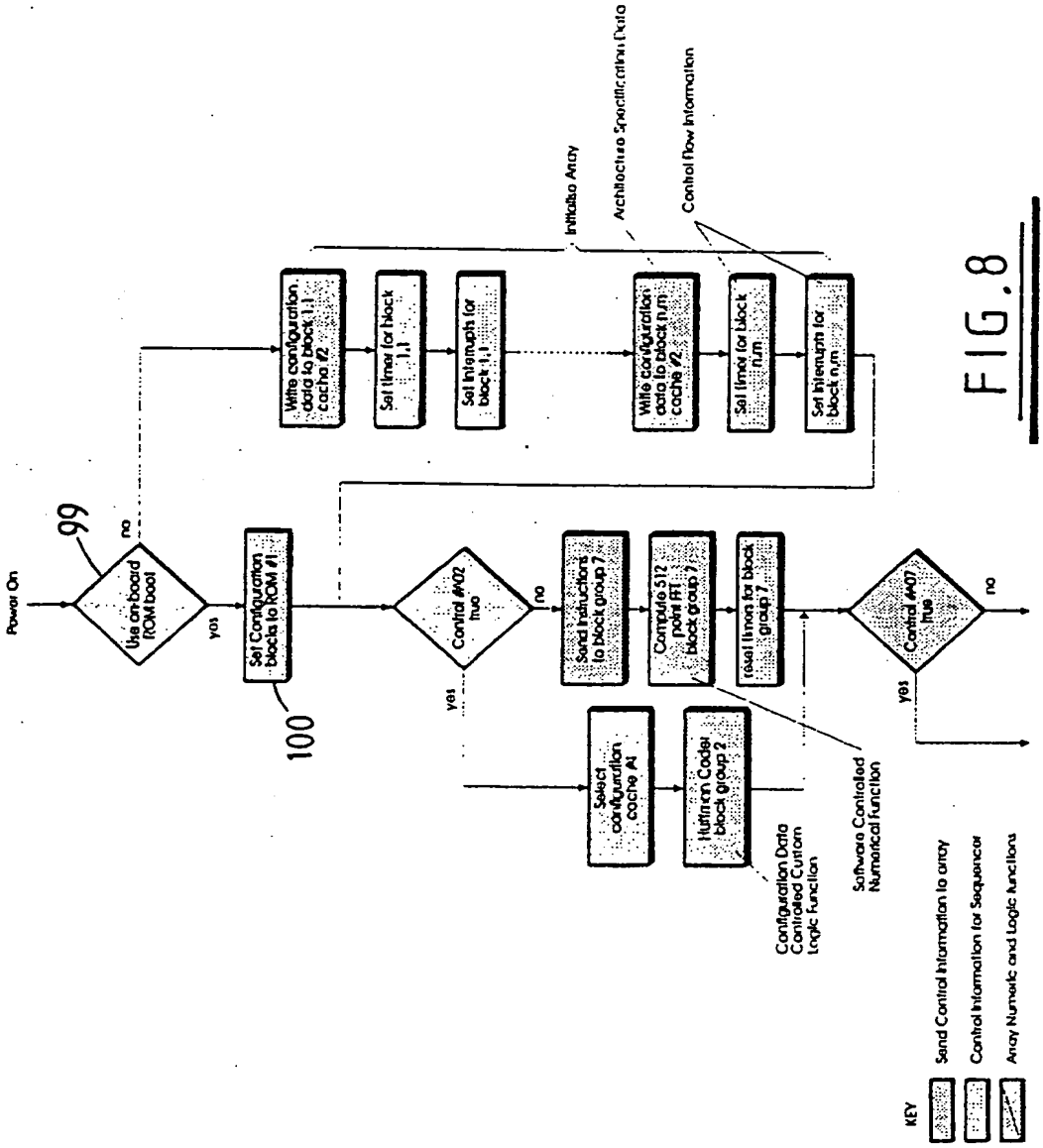
Initialize Array
Architecture Specification Data
Control flow information
Write configuration data to block 1,1 cache #2
Set timer for block 1,1
Set interrupts for block 1,1
Write configuration data to block n,m cache #2
Set timer for block n,m
Set interrupts for block n,m
Power On
99
Use on board ROM boot
no
yes
Set Configuration blocks to ROM #1
100
Control #402 true
no
yes
Send instructions to block group 7
Compute 512 point FFT block group 7
reset timers for block group 7
Control #407 true
no
yes
Select configuration cache #1
Huffman Coder block group 2
Configuration Data Controlled Custom Logic Function
Software Controlled Numerical function
KEY
Send Control information to array
Control information for Sequencer
Array Numeric and Logic functions

FIG. 8

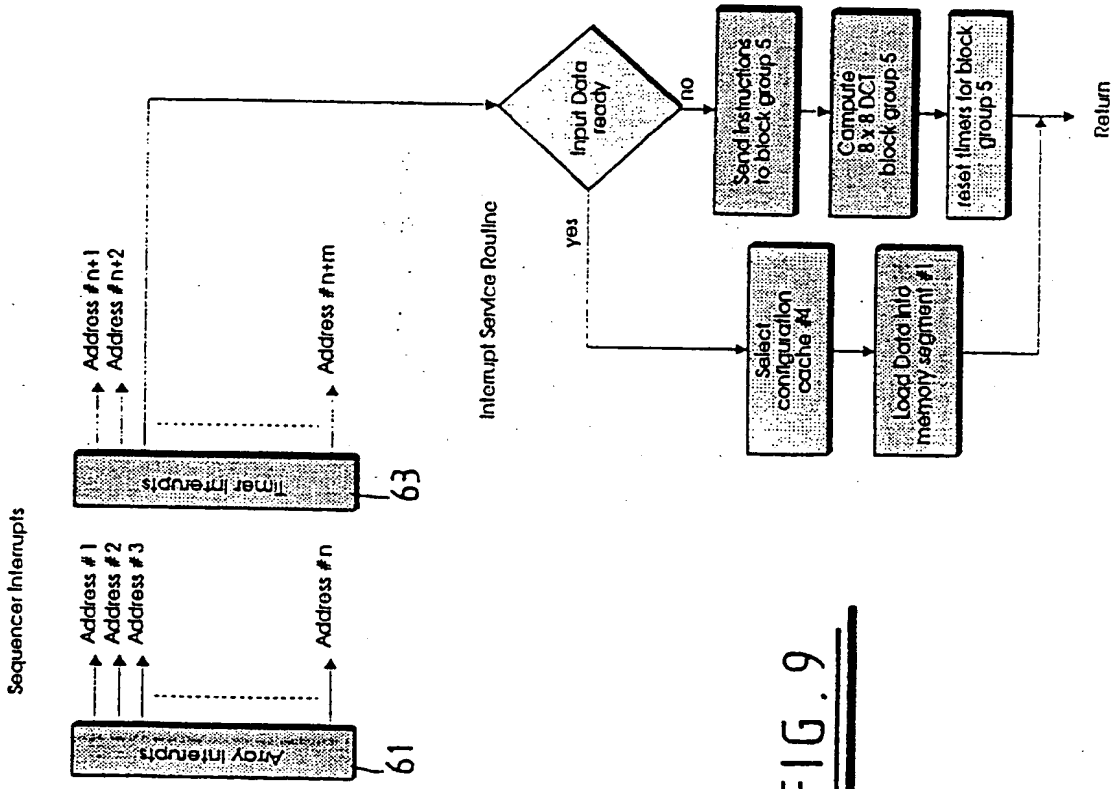
Sequencer Interrupts
Array Interrupts
Address #1
Address #2
Address #3
Address #n
61
Timer Interrupts
Address #n+1
Address #n+2
Address #n+m
63
Interrupt Service Routine
Input Data ready
no
yes
Send instructions to block group 5
Compute 8 x 8 DCT block group 5
Reset timers for block group 5
Return
Select configuration cache #4
Load Data into memory segment #1

FIG. 9

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/GB 96/02013

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F15/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP,A,0 637 173 (HITACHI LTD) 1 February 1995 see page 3, line 16 - line 20 see page 3, line 37 - line 46 see page 4, line 45 - page 5, line 58 see page 7, line 10 - line 21 see figures 1,2,4,5,16	1-4
A	EP,A,0 497 029 (ANALOGIC CORP) 5 August 1992 see the whole document	1

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Date of the actual completion of the international search	Date of mailing of the international search report
6 December 1996	19. 12. 96

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Information on patent family members

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PCT/GB 96/02013

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0637173	01-02-95	JP-A-	7036858	07-02-95
		US-A-	5537601	16-07-96
EP-A-0497029	05-08-92	US-A-	5301344	05-04-94
		JP-A-	6131155	13-05-94
		JP-B-	7101381	01-11-95

DOCKET NO: GR98P8107
SERIAL NO: 09/816,926
APPLICANT: Arnold et al.

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